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2016-2017 VLSI PROJECTS LIST

S.NO	PROJECT TITLE	VERTICAL
1.	A FULLY DIGITAL FRONT-END ARCHITECTURE FOR ECG ACQUISITION SYSTEM WITH 0.5 V SUPPLY	VLSI
2.	LOW-COST HIGH-PERFORMANCE VLSI ARCHITECTURE FOR MONTGOMERY MODULAR MULTIPLICATION	VLSI
3.	RF POWER GATING: A LOW-POWER TECHNIQUE FOR ADAPTIVE RADIOS	VLSI
4.	LOW-POWER ECG-BASED PROCESSOR FOR PREDICTING VENTRICULAR ARRHYTHMIA	VLSI
5.	A NEW PARALLEL VLSI ARCHITECTURE FOR REAL-TIME ELECTRICAL CAPACITANCE TOMOGRAPHY	VLSI
6.	LOW-POWER FPGA DESIGN USING MEMOIZATION-BASED APPROXIMATE COMPUTING	VLSI
7.	LOW-POWER SPLIT-RADIX FFT PROCESSORS USING RADIX-2 BUTTERFLY UNITS	VLSI
8.	A HIGH-SPEED FPGA IMPLEMENTATION OF AN RSD-BASED ECC PROCESSOR	VLSI
9.	HIGH-SPEED AND ENERGY-EFFICIENT CARRY SKIP ADDER OPERATING UNDER A WIDE RANGE OF SUPPLY VOLTAGE LEVELS	VLSI

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10.	A 0.52/1 V FAST LOCK-IN ADPLL FOR SUPPORTING DYNAMIC VOLTAGE AND FREQUENCY SCALING	VLSI
11.	CODE COMPRESSION FOR EMBEDDED SYSTEMS USING SEPARATED DICTIONARIES	VLSI
12.	A DYNAMICALLY RECONFIGURABLE MULTI-ASIP ARCHITECTURE FOR MULTI-STANDARD AND MULTIMODE TURBO DECODING	VLSI
13.	DESIGN AND IMPLEMENTATION OF HIGH-SPEED ALL-PASS TRANSFORMATION-BASED VARIABLE DIGITAL FILTERS BY BREAKING THE DEPENDENCE OF OPERATING FREQUENCY ON FILTER ORDER	VLSI
14.	A MIXED-DECIMATION MDF ARCHITECTURE FOR RADIX-2K PARALLEL FFT	VLSI
15.	ALGORITHM AND ARCHITECTURE OF CONFIGURABLE JOINT DETECTION AND DECODING FOR MIMO WIRELESS COMMUNICATIONS WITH CONVOLUTION CODES	VLSI
16.	ONE-CYCLE CORRECTION OF TIMING ERRORS IN PIPELINES WITH STANDARD CLOCKED ELEMENTS	VLSI
17.	HARDWARE AND ENERGY-EFFICIENT STOCHASTIC LU DECOMPOSITION SCHEME FOR MIMO RECEIVERS	VLSI
18.	HYBRID LUT/MULTIPLEXER FPGA LOGIC ARCHITECTURES	VLSI
19.	A 520K (18 900, 17 010) ARRAY DISPERSION LDPC DECODER ARCHITECTURES FOR NAND-FLASH MEMORY	VLSI
20.	IMPLEMENTING MINIMUM-ENERGY-POINT SYSTEMS WITH ADAPTIVE LOGIC	VLSI

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21.	HIGH-PERFORMANCE PIPELINED ARCHITECTURE OF ELLIPTIC CURVE SCALAR MULTIPLICATION OVER GF(2M)	VLSI
22.	HIGH-PERFORMANCE NB-LDPC DECODER WITH REDUCTION OF MESSAGE EXCHANGE	VLSI
23.	LUT OPTIMIZATION FOR DISTRIBUTED ARITHMETIC-BASED BLOCK LEAST MEAN SQUARE ADAPTIVE FILTER	VLSI
24.	GRAPH-BASED TRANSISTOR NETWORK GENERATION METHOD FOR SUPERGATE DESIGN	VLSI
25.	FLEXIBLE DSP ACCELERATOR ARCHITECTURE EXPLOITING CARRY-SAVE ARITHMETIC	VLSI
26.	A CELLULAR NETWORK ARCHITECTURE WITH POLYNOMIAL WEIGHT FUNCTIONS	VLSI
27.	A HIGH-PERFORMANCE FIR FILTER ARCHITECTURE FOR FIXED AND RECONFIGURABLE APPLICATIONS	VLSI
28.	FAULT TOLERANT PARALLEL FFTS USING ERROR CORRECTION CODES AND PARSEVAL CHECKS	VLSI
29.	EXPLOITING INTRACELL BIT-ERROR CHARACTERISTICS TO IMPROVE MIN-SUM LDPC DECODING FOR MLC NAND FLASH-BASED STORAGE IN MOBILE DEVICE	VLSI
30.	UNEQUAL-ERROR-PROTECTION ERROR CORRECTION CODES FOR THE EMBEDDED MEMORIES IN DIGITAL SIGNAL PROCESSORS	VLSI
31.	A HIGH THROUGHPUT LIST DECODER ARCHITECTURE FOR POLAR CODES	VLSI

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32.	A NORMAL I/O ORDER RADIX-2 FFT ARCHITECTURE TO PROCESS TWIN DATA STREAMS FOR MIMO	VLSI
33.	DESIGN AND FPGA IMPLEMENTATION OF A RECONFIGURABLE 1024-CHANNEL CHANNELIZATION ARCHITECTURE FOR SDR APPLICATION	VLSI
34.	INPUT-BASED DYNAMIC RECONFIGURATION OF APPROXIMATE ARITHMETIC UNITS FOR VIDEO ENCODING	VLSI
35.	A CONFIGURABLE PARALLEL HARDWARE ARCHITECTURE FOR EFFICIENT INTEGRAL HISTOGRAM IMAGE COMPUTING	VLSI
36.	A NEW BINARY-HALVED CLUSTERING METHOD AND ERT PROCESSOR FOR ASSR SYSTEM	VLSI
37.	THE VLSI ARCHITECTURE OF A HIGHLY EFFICIENT DE-BLOCKING FILTER FOR HEVC SYSTEMS	VLSI
38.	LOW-POWER SYSTEM FOR DETECTION OF SYMPTOMATIC PATTERNS IN AUDIO BIOLOGICAL SIGNALS	VLSI
39.	IN-FIELD TEST FOR PERMANENT FAULTS IN FIFO BUFFERS OF NOC ROUTERS	VLSI
40.	SOURCE CODE ERROR DETECTION IN HIGH-LEVEL SYNTHESIS FUNCTIONAL VERIFICATION	VLSI
41.	A SINGLE-ENDED WITH DYNAMIC FEEDBACK CONTROL 8T SUBTHRESHOLD SRAM CELL	VLSI
42.	OTA-BASED LOGARITHMIC CIRCUIT FOR ARBITRARY INPUT SIGNAL AND ITS APPLICATION	VLSI

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43.	A ROBUST ENERGY/AREA-EFFICIENT FORWARDED-CLOCK RECEIVER WITH ALL-DIGITAL CLOCK AND DATA RECOVERY IN 28-NM CMOS FOR HIGH-DENSITY INTERCONNECTS	VLSI
44.	FULL-SWING LOCAL BITLINE SRAM ARCHITECTURE BASED ON THE 22-NM FINFET TECHNOLOGY FOR LOW-VOLTAGE OPERATION	VLSI
45.	A 0.1–3.5-GHZ DUTY-CYCLE MEASUREMENT AND CORRECTION TECHNIQUE IN 130-NM CMOS	VLSI
46.	A LOW-POWER ROBUST EASILY CASCADED PENTAMTJ-BASED COMBINATIONAL AND SEQUENTIAL CIRCUITS	VLSI
47.	LOW-POWER VARIATION-TOLERANT NONVOLATILE LOOKUP TABLE DESIGN	VLSI
48.	LOW-ENERGY POWER-ON-RESET CIRCUIT FOR DUAL SUPPLY SRAM	VLSI
49.	FREQUENCY-BOOST JITTER REDUCTION FOR VOLTAGE-CONTROLLED RING OSCILLATORS	VLSI
50.	HIGH-SPEED, LOW-POWER, AND HIGHLY RELIABLE FREQUENCY MULTIPLIER FOR DLL-BASED CLOCK GENERATOR	VLSI
51.	A SYSTEMATIC DESIGN METHODOLOGY OF ASYNCHRONOUS SAR AD	VLSI
52.	READ BIT LINE SENSING AND FAST LOCAL WRITE-BACK TECHNIQUES IN HIERARCHICAL BITLINE ARCHITECTURE FOR ULTRALOW-VOLTAGE SRAMS	VLSI
53.	ONLINE MEASUREMENT OF DEGRADATION DUE TO BIAS TEMPERATURE INSTABILITY IN SRAMS	VLSI

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54.	INCORPORATING PROCESS VARIATIONS INTO SRAM ELECTROMIGRATION RELIABILITY ASSESSMENT USING ATOMIC FLUX DIVERGENCE	VLSI
55.	EMDBAM: A LOW-POWER DUAL BIT ASSOCIATIVE MEMORY WITH MATCH ERROR AND MASK CONTROL	VLSI
56.	A SINGLE-STAGE LOW-DROPOUT REGULATOR WITH A WIDE DYNAMIC RANGE FOR GENERIC APPLICATIONS	VLSI
57.	GLITCH ENERGY REDUCTION AND SFDR ENHANCEMENT TECHNIQUES FOR LOW-POWER BINARY-WEIGHTED CURRENT-STEERING DAC	VLSI
58.	INTEGRATED FLOATING-GATE PROGRAMMING ENVIRONMENT FOR SYSTEM-LEVEL ICS	VLSI
59.	DESIGN OF SILICON PHOTONIC INTERCONNECT ICS IN 65-NM CMOS TECHNOLOGY	VLSI
60.	TEST ESCAPES OF STUCK-OPEN FAULTS CAUSED BY PARASITIC CAPACITANCES AND LEAKAGE CURRENTS	VLSI
61.	STATISTICAL FRAMEWORK AND BUILT-IN SELF SPEED-BINNING SYSTEM FOR SPEED BINNING USING ON-CHIP RING OSCILLATORS	VLSI
62.	A LOW-POWER BROAD-BANDWIDTH NOISE CANCELLATION VLSI CIRCUIT DESIGN FOR IN-EAR HEADPHONES	VLSI
63.	A 3-D CPU-FPGA-DRAM HYBRID ARCHITECTURE FOR LOW-POWER COMPUTATION	VLSI
64.	LOW-POWER/COST RNS COMPARISON VIA PARTITIONING THE DYNAMIC RANGE	VLSI

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65.	DESIGN OF A NETWORK OF DIGITAL SENSOR MACROS FOR EXTRACTING POWER SUPPLY NOISE PROFILE IN SOCS	VLSI
66.	UNDERSTANDING THE RELATION BETWEEN THE PERFORMANCE AND RELIABILITY OF NAND FLASH/SCM HYBRID SOLID-STATE DRIVE	VLSI
67.	FCUDA-NOC : A SCALABLE AND EFFICIENT NETWORK-ON-CHIP IMPLEMENTATION FOR THE CUDA-TO-FPGA FLOW	VLSI
68.	OPTIMIZED BUILT-IN SELF-REPAIR FOR MULTIPLE MEMORIES	VLSI
69.	MEASURING IMPROVEMENT WHEN USING HUB FORMATS TO IMPLEMENT FLOATING-POINT SYSTEMS UNDER ROUND-TO-NEAREST	VLSI
70.	FLEXIBLE ECC MANAGEMENT FOR LOW-COST TRANSIENT ERROR PROTECTION OF LAST-LEVEL CACHES	VLSI
71.	SOURCE CODING AND PREEMPHASIS FOR DOUBLE-EDGED PULSE WIDTH MODULATION SERIAL COMMUNICATION	VLSI
72.	A HIGH-THROUGHPUT HARDWARE DESIGN OF A ONE-DIMENSIONAL SPIHT ALGORITHM	VLSI
73.	NETWORK-ON-CHIP FOR TURBO DECODERS	VLSI
74.	ENHANCED WEAR-RATE LEVELING FOR PRAM LIFETIME IMPROVEMENT CONSIDERING PROCESS VARIATION	VLSI
75.	SPECULATIVE LOOK AHEAD FOR ENERGY-EFFICIENT MICROPROCESSORS	VLSI

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76.	A REAL-TIME NETWORK-ON-CHIP ARCHITECTURE WITH AN EFFICIENT GALS IMPLEMENTATION	VLSI
77.	EFFICIENT DYNAMIC VIRTUAL CHANNEL ORGANIZATION AND ARCHITECTURE FOR NOC SYSTEMS	VLSI
78.	EFFICIENT SYNCHRONIZATION FOR DISTRIBUTED EMBEDDED MULTIPROCESSORS	VLSI
79.	NAND FLASH MEMORY WITH MULTIPLE PAGE SIZES FOR HIGH-PERFORMANCE STORAGE DEVICES	VLSI
80.	A PERFORMANCE DEGRADATION TOLERABLE CACHE DESIGN BY EXPLOITING MEMORY HIERARCHIES	VLSI
81.	KNOWLEDGE-BASED NEURAL NETWORK MODEL FOR FPGA LOGICAL ARCHITECTURE DEVELOPMENT	VLSI
82.	ENERGY-EFFICIENT FLOATING-POINT MFCC EXTRACTION ARCHITECTURE FOR SPEECH RECOGNITION SYSTEMS	VLSI
83.	A NEW OPTIMAL ALGORITHM FOR ENERGY SAVING IN EMBEDDED SYSTEM WITH MULTIPLE SLEEP MODES	VLSI
84.	A FAST FAULT-TOLERANT ARCHITECTURE FOR SAUVOLA LOCAL IMAGE THRESHOLDING ALGORITHM USING STOCHASTIC COMPUTING	VLSI
85.	EFFICIENCY ENABLERS OF LIGHTWEIGHT SDR FOR MIMO BASEBAND PROCESSING	VLSI
86.	A NOVEL QUANTUM-DOT CELLULAR AUTOMATA X-BIT ×32-BIT SRAM	VLSI

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87.	GPU-ACCELERATED PARALLEL SPARSE LU FACTORIZATION METHOD FOR FAST CIRCUIT ANALYSIS	VLSI
88.	ULTRALOW-ENERGY VARIATION-AWARE DESIGN: ADDER ARCHITECTURE STUDY	VLSI
89.	AN ALL-DIGITAL APPROACH TO SUPPLY NOISE CANCELLATION IN DIGITAL PHASE-LOCKED LOOP	VLSI
90.	WRITE BUFFER-ORIENTED ENERGY REDUCTION IN THE L1 DATA CACHE FOR EMBEDDED SYSTEMS	VLSI
91.	PROCESS VARIATION DELAY AND CONGESTION AWARE ROUTING ALGORITHM FOR ASYNCHRONOUS NOC DESIGN	VLSI
92.	TOWARD SOLVING MULTICHANNEL RF-SOC INTEGRATION ISSUES THROUGH DIGITAL FRACTIONAL DIVISION	VLSI
93.	ERROR RESILIENT AND ENERGY EFFICIENT MRF MESSAGE-PASSING-BASED STEREO MATCHING	VLSI
94.	FLOATING-POINT BUTTERFLY ARCHITECTURE BASED ON BINARY SIGNED-DIGIT REPRESENTATION	VLSI
95.	ON EFFICIENT RETIMING OF FIXED-POINT CIRCUITS	VLSI
96.	A FAST-ACQUISITION ALL-DIGITAL DELAY-LOCKED LOOP USING A STARTING-BIT PREDICTION ALGORITHM FOR THE SUCCESSIVE-APPROXIMATION REGISTER	VLSI
97.	DESIGN OF MODIFIED SECOND-ORDER FREQUENCY TRANSFORMATIONS BASED VARIABLE DIGITAL FILTERS WITH LARGE CUTOFF FREQUENCY RANGE AND IMPROVED TRANSITION BAND CHARACTERISTICS	VLSI

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98.	FIXED-POINT COMPUTING ELEMENT DESIGN FOR TRANSCENDENTAL FUNCTIONS AND PRIMARY OPERATIONS IN SPEECH PROCESSING	VLSI
99.	TRIGGER-CENTRIC LOOP MAPPING ON CGRAS	VLSI
100.	AREA-AWARE CACHE UPDATE TRACKERS FOR POST SILICON VALIDATION	VLSI